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Low-power nanophotonic devices based on photonic crystals towards dense photonic network on chip

M. Notomi[1] *A. Shinya*[1] *K. Nozaki*[1] *T. Tanabe*[1] *S. Matsuo*[2] *E. Kuramochi*[1] *T. Sato*[2] *H. Taniyama*[1] *H. Sumikura*[1]

[1]*NTT Basic Research Laboratories, NTT Corporation, 3-1 Morinosato-Wakamiya, Atsugi 243-0198, Japan*
[2]*NTT Photonics Laboratories, NTT Corporation, 3-1 Morinosato-Wakamiya, Atsugi 243-0198, Japan*
E-mail: notomi@nttbrl.jp

Abstract: The authors review their recent studies on various nanophotonic devices including all-optical switches, optical memories, electro-optic modulators, photo-detectors and lasers, all of which are based on photonic crystal (PhC) nanocavities. The strong light confinement achieved in PhC nanocavities has enabled these devices with ultrasmall footprint and ultralow power/energy consumption. These characteristics are ideally suited for constructing dense photonic network on chip, which will overcome the limitation of future CMOS chips in terms of high-speed operation with less energy consumption and heat generation.

1 Introduction

It is widely recognised that the various stages of information processing including MPUs (microprocessor units), network routers and data centres are now facing the same problem, namely, they consume too much energy and generate heat when operating at high-bit rate. This is hampering further increase in bandwidth and also threatening the global environment [1–3]. Most of the energy required for high-speed data processing is now consumed by the electronic data transport in processing nodes (board-to-board, chip-to-chip or core-to-core) [4]. In fact, today's high-speed network has been built by replacing copper electric cables with optical glass fibres. This success proves that photonics is superior to electronics with respect to long-haul data transport. Now, it is expected that the introduction of photonics into much shorter length scale (that is, into processing nodes) will be a solution for the present problem. This is because photonic data transport does not require a large amount of energy even for high-bit rate data. Naturally, the introduction of photonics has been started board-to-board, and is now being expanded to chip-to-chip. Such simple optical interconnect technologies are currently extensively studied. The intra-chip optical interconnection is also being discussed although it is still not concreted yet when it will be installed [3]. For the chip-scale optical interconnect, it has been proposed and discussed that it will be advantageous to introduce sophisticated optical networking technologies (that has been developed for optical communication) instead of simple interconnect. This is sometimes referred to as a photonic network on chip and abbreviated as photonic NoC or PhNoC [5]. In this article, we concentrate on the ultimate embodiment of chip-scale optical interconnect where we employ dense PhNoC technologies because we believe that such technology will be finally required in future.

Fig. 1 is a schematic of an example of the possible photonic NoC configurations, where a photonic network layer is overlaid on a CMOS electronic circuit in the same chip. Although the details of the photonic network layer have not yet been concreted, we obviously need a large number of various types of photonic devices (lasers, detectors, switches etc.) integrated via waveguides in a chip for photonic NoC. Since the photonic layer should be comparable in size to the CMOS circuit, the size and energy consumption of these photonic devices should be extremely small while maintaining a high-bit rate operation. For MPU applications [3], the energy cost for single-bit data transport should be <10 fJ/bit, and the required number of the transport channels will be an order of 10^4 or more. When we pursue higher-bit rate, the photonic layer should become much denser.

However, conventional photonic devices do not meet such requirements. They are generally large (100 μm to 1 mm), consume a large amount of energy per bit operation (pJ/bit or more) and are difficult to integrate in a chip (examples for conventional lasers are given in [6, 7], and examples for conventional optical switches are given in [8–28]). Simple mathematics shows that if we integrate 10^4 devices operating at 100 Gbps with an energy consumption of 1 pJ/bit, the photonic layer would consume at least 1 kW, and the size would be 100 cm^2 or more. Moreover, since photonic integration technologies are not yet mature, the integrated size including waveguides would be even much larger in order of magnitude than 100 cm^2. Thus, it is apparent that the degree of integrity for the photonic layer will be severely restricted by this problem. If we really

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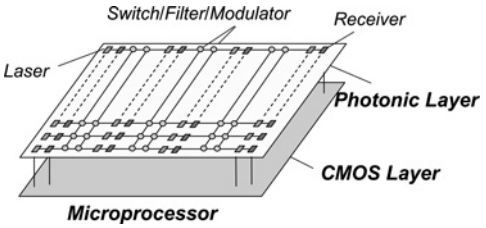

Fig. 1 *Photonic NoC*

require dense PhNoC, obviously we need some novel photonic devices that are fundamentally different from those now in use. These might be functional nanophotonic devices that are easily integratable and that can operate with an energy of fJ/bit.

2 Impact of photonic crystal nanocavities for dense photonic NoC

The device requirements for photonic NoC are not easy to meet. The reason for this can be attributed to the fundamental nature of light in materials, namely that light is difficult to confine for a long time in a small volume. Electrons are easily confined by applying a voltage or by implementing a potential barrier, but photons are not. We have to use some kind of reflection to confine photons, but conventional reflection is not effective for this purpose. Reflection at a metal mirror is accompanied by an inevitable absorption loss of several percent, which is too large for strong light confinement. Total internal reflection at a boundary separating media with different refractive indices is generally employed for constructing photonic components, but it becomes ineffective when the confinement size is comparable to optical wavelength. In other words, it has been difficult to construct very high-Q optical cavities with a size comparable to optical wavelengths by conventional methods. This fact makes it difficult to construct nanophotonic devices for photonic NoC.

Recently, there has been a breakthrough as regards light confinement. It has been demonstrated that an artificial structure whose refractive index is periodically modulated, namely a photonic crystal (PhC) [29, 30], can confine light very strongly. An example PhC is shown in Fig. 2*a*. The concept of PhCs and their ability of strong light confinement was theoretically proposed more than two decades ago [31, 32], and many research activities have been conducted since then. However, it was just recently that the strong light confinement was realised and ultrasmall-and-ultrahigh-Q cavities (an effective cavity mode volume V_{eff} of $\sim(\lambda/n)^3$ and $Q > 10^6$) were produced in PhCs [33–37]. An example of such cavities is shown in Figs. 2*b*–*d*. The periodic part of this structure has a photonic band gap (PBG). If the frequency lies inside the PBG, light propagation is prohibited (thus, such PhCs are sometimes referred to as 'photonic insulators'). This confinement mechanism is effective even when the size becomes comparable to the wavelength of light and it is not accompanied by a loss if the structure is perfect. Thus, PBG can confine light in a volume comparable to optical wavelengths for a long time.

Since high-quality three-dimensional (3D) PBG is still difficult, these ultrahigh-Q cavities have been realised in 2D PhCs with 2D PBGs. It has been found and demonstrated that the vertical (out-of-plane) radiation loss from 2D PhCs can be substantially reduced by employing sophisticated designs. The cavity shown in Figs. 2*b*–*d* [34, 36] is based on a line-defect waveguide which is known to be free of radiation loss. A slight structural modulation of the waveguide (the shaded holes are shifted outwards by 3–9 nm) produces a cavity mode in the centre region. This is an example of modulated mode-gap cavity designs that have been studied in various forms recently in many research groups [34, 38]. We confirmed that our design can realise a theoretical $Q > 10^8$ with V_{cav} is $\sim(\lambda/n)^3$. Figs. 2e and f shows experimental results for this particular cavity fabricated in silicon PhCs by electron-beam lithography and dry etching. The cavity is integrated with input/output waveguides. The optical transmission spectrum (Fig. 2*e*) exhibits an ultrasharp resonance peak which corresponds to a cavity Q of 1.8×10^6. Fig. 2*f* shows a time-resolved ring-down measurement that reveals the monotonic exponential decay of light trapped in the cavity with a photon lifetime of 1.5 ns. This value corresponds to a cavity Q of 1.8×10^6 that is exactly the same as the result obtained from Fig. 2*e*.

In terms of photonic NoC applications, the important features of these PhC nanocavities can be summarised as follows.

2.1 High Q and small V_{cav}

At present, no cavities other than those based on PhCs have achieved a Q higher than 10^2 and V_{cav} $\sim(\lambda/n)^3$, simultaneously. If we are allowed to relax size constraints, toroidal cavities have achieved $Q > 10^8$, but the toroid diameter is several hundreds of μm or more [39]. If we can sacrifice Q, plasmonic cavities have achieved $V_{\text{cav}} \sim 0.01\ \mu\text{m}^3$ [40], but the Q value is limited to just a few tens. As explained later, the ratio Q/V_{cav} represents the degree of light–matter interaction enhancement in cavities, which eventually leads to reduced energy consumption in photonic devices. Thus, a large Q/V_{cav} in PhC nanocavities is very important for reducing the energy consumption of photonic devices [30]. Of course, smaller V_{cav} itself means a smaller device size. Thus, high-Q and small-V_{cav} cavities may simultaneously solve two problems in photonic devices, namely their large footprint and high energy consumption.

2.2 Integratability

Another even more important feature of PhC cavities is their ability of integration. Generally, it is difficult to install many photonic devices in the same chip and connect them effectively. If we strongly confine light in devices, it makes it more difficult to establish effective connections. Thus, conventional high-Q cavities, such as micro-ring cavities, whispering-gallery cavities and micro-post cavities are difficult to integrate with waveguides. In contrast, the cavity in Fig. 2 is already integrated with input/output waveguides. It is easy and straightforward to integrate PhC cavities with waveguides, and the cavity–waveguide coupling strength can be accurately controlled by employing an appropriate PhC design. In fact, there have been many proposals and demonstrations of the integration of multiple PhC cavities via waveguides in a single chip [41]. We have reported an experimental demonstration of multi-port drop filters consisting of five different cavities [42]. More recently, we have reported the successful fabrication of a large-scale array of coupled PhC cavities, in which 200 (later increased to 400) ultrahigh-Q nanocavities (the design is the same as that in Fig. 2) are coupled to form slow light bands [43].

For these reasons, we believe that PhC nanocavities are promising candidates for realising photonic NoC. Currently,

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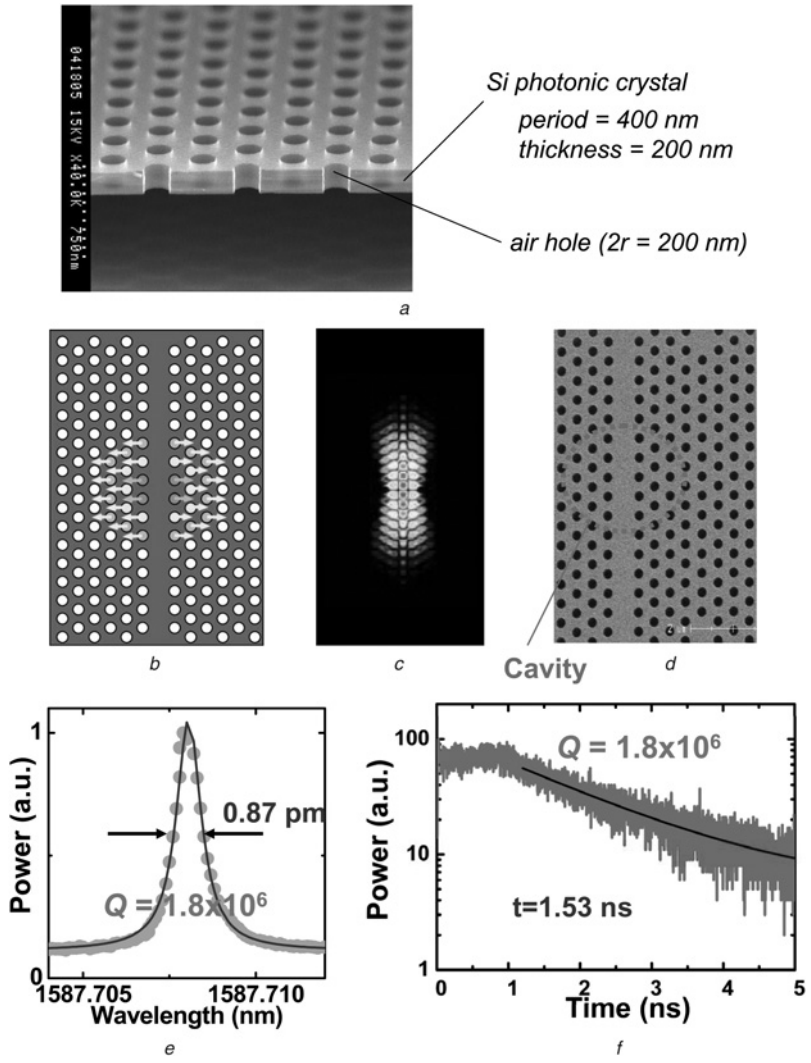

Fig. 2 PhC*s and nanocavities*

a Scanning electron micrograph of a Si PhC (hexagonal air-hole array)
b Structural design of a width-modulated line-defect nanocavity. Shaded holes are shifted outwards by 3–9 nm
c Calculated light-field profile of the cavity in *b*
d Scanning electron micrograph of a width-modulated line-defect cavity coupled with input/output waveguides in a Si PhC
e Measured transmission spectrum
f Time-resolved ring-down measurement

we are conducting a series of studies of several different nanophotonic devices based on PhC nanocavities. The following sections provide a brief summary of these studies.

3 All-optical switch

As a first example of nanophotonic devices based on PhCs, we examine an all-optical switch, which is a typical and very straightforward example of light–matter interaction enhancement by nanocavities [37]. As shown in Fig. 3*a*, this device switches the optical intensity output from the device by applying another control optical pulse. Although there are many different variations, most of them are based on interferometers or resonators in which the interference or resonant condition is shifted via the optical third-order non-linearity [$\chi^{(3)}$] of materials [that is, the non-linear (NL) refractive index]. The operating principle of resonator-based switches is shown in Fig. 3*c*. Since optical non-linearity is generally very weak, we need to input relatively high power into the switches for operation, and the device size tends to become larger so as to increase the interaction length. Normal all-optical switches based on NL waveguide interferometers are at least a millimetre long with a pJ/bit or greater energy consumption.

The switching energy U_{sw} for all-optical switches based on resonators is determined by the relations $1/Q = \Delta n/n$, $\Delta n = 2n_2|E|^2$ and $U = \varepsilon_0\varepsilon|E|^2V_{cav}/2$ [44], where n is the refractive index and Δn is the NL index shift, and is generally given by

$$U_{sw} = \frac{\varepsilon_0 \varepsilon n}{2n_2}\frac{V_{cav}}{Q} \tag{1}$$

where n_2 is the NL refractive index. This equation clearly shows that when Q/V_{cav} is large, the switching energy can be reduced in proportion to V_{cav}/Q. Hence, if we employ a small photonic crystal nanocavity with high-Q containing appropriate optical NL material, we will be able to realise a wavelength-sized switch requiring only small driving energy.

There are various types of optical non-linearity, including the Kerr effect, carrier-induced non-linearity and thermo-optic non-linearity. Of these, carrier-induced non-linearity

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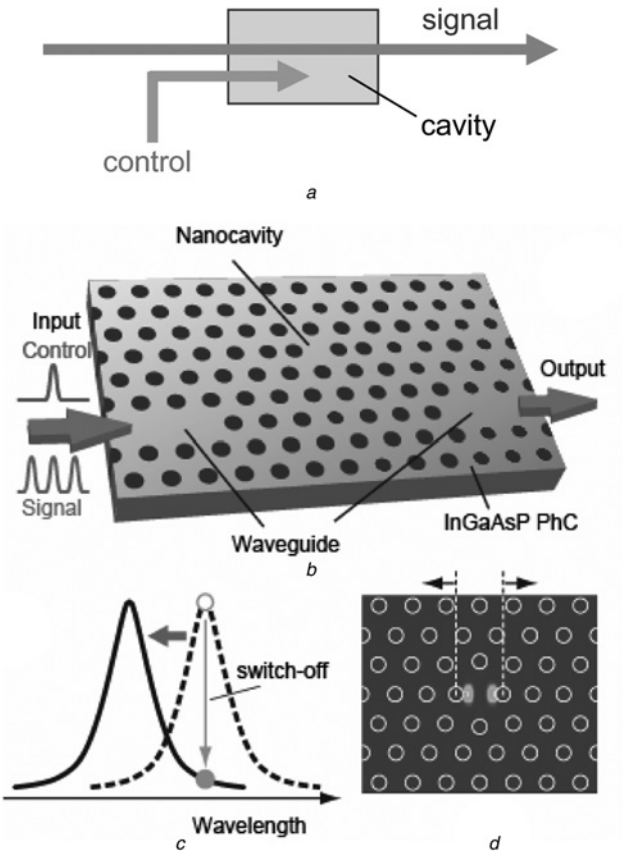

Fig. 3 *Schematics of all-optical switch based on an ultrasmall* PhC *nanocavity*

a Schematic of all-optical switch
b Structural design of all-optical switch in an InGaAsP PhC
c Operating principle of all-optical switch
d Design of an ultrasmall nanocavity and calculated light-field profile of the cavity

(namely, non-linearity based on real transition) generally exhibits the largest n_2, but it always suffers from slow switching speed because it is restricted by the generally slow carrier relaxation time. However, if we employ an ultrasmall cavity, the carrier relaxation time can be greatly shortened. This is because the generated carriers escape rapidly from the nanocavity as a result of carrier diffusion [37]. As is generally known, diffusion becomes faster when the initial distribution is concentrated in a smaller volume. This mechanism is very efficient in semiconductors with high mobility, such as Si, GaAs or InP-based compound semiconductors, which also have large n_2. As regards carrier-induced non-linearity, the switching energy is deduced from the relations $1/Q = \Delta n/n$, $\Delta n = \sigma N$ and $U = N\eta\omega_{\text{pump}}$, and is given by

$$U_{\text{sw}} \simeq \frac{2n}{\sigma}\frac{V_{\text{cav}}}{Q}\hbar\omega_{\text{pump}} \tag{2}$$

where σ is the carrier-induced index shift coefficient [45] and N is the carrier density generated by optical pumping. We assumed the critical coupling condition which corresponds to the situation where half of the pump light is absorbed in the cavity.

Against this background, we demonstrated all-optical switching at telecommunication wavelengths ($\sim$1.55 μm) in silicon PhCs in 2005 [46]. The switch consists of a nanocavity (so-called L4 cavity) with $Q = 10^4$ and $V_{\text{cav}} = 0.07\ \mu\text{m}^3$. Although Si is transparent at 1.55 μm, carriers can be generated via the two-photon absorption (TPA) process. We made use of a combination of TPA and carrier-plasma dispersion in Si for achieving optical non-linearity. The switching energy and time were 200 fJ/bit and approximately 100 ps, respectively. The observed switching energy and time were both an order of magnitude smaller than those in other all-optical Si switches based on the same NL mechanism. Besides our work, there have been several reports of applying PhCs for all-optical switches in various forms [47–50].

Recently, we applied the same idea to much smaller nanocavities in InGaAsP PhCs (Fig. 3*b*) [51]. The switch consists of a so-called hole-shifted cavity (shown in Fig. 3*d*, and is also called an H0 cavity) which has the smallest cavity mode volume ($V_{\text{cav}} = 0.025\ \mu\text{m}^3$) among dielectric-core cavities [52, 53]. In addition, the NL index shift in InGaAsP is several 10 times larger than that in Si at 1.55 μm if the composition is optimised. The measured switching dynamics of the device is shown in Fig. 4*a*. The achieved switching energies were 420 and 660 aJ for contrasts of 3 and 10 dB, respectively, with a switching time window of 20–40 ps. The improvement in energy and speed is attributed to the smallness of the cavity and the large non-linearity of InGaAsP. As far as we know, this is the smallest switching energy reported for all-optical switches, and is the first sub-fJ/bit all-optical switching operation. Fig. 4*b* compares of various all-optical switches in terms of their switching energy per bit and switching time window. As clearly seen in Fig. 4*b*, the present all-optical switch can operate with approximately two or more

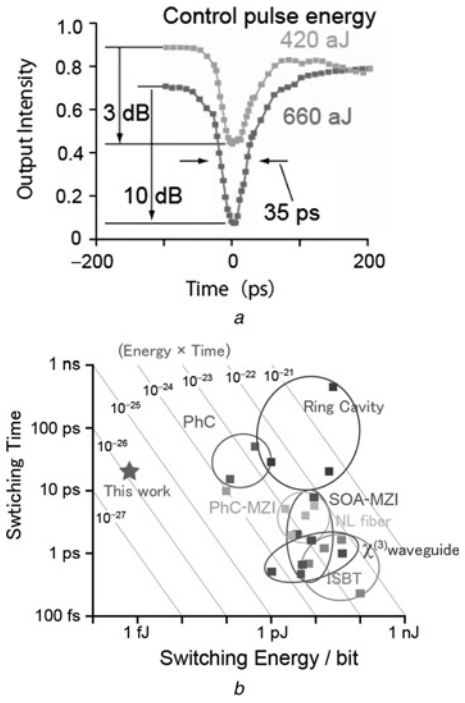

Fig. 4 *Low-energy operation of all-optical switch*

a Measured switching dynamics of all-optical switch based on an ultrasmall InGaAsP PhC nanocavity under two different control pulse energy conditions
b Comparison of the switching energy per bit and switching time window for various all-optical switches
The data were taken from the following references. [46–48] for PhC switches, [8–10] for ring cavity switches, [11–13] for laser diode switches, [14–17] for semiconductor optical amplifier Mach-Zehnder interferometer switches, [18–21] for NL fibre switches, [22–24] for $\chi^{(3)}$ waveguide switches, and [25–28] for inter-subband transition switches

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orders of magnitude less energy. Note that we did not sacrifice the switching speed to achieve this energy reduction, which can be attributed to the fact that we employed ultrasmall cavities. In these all-optical switches, as the cavity size becomes smaller, both the switching energy and switching time are reduced.

4 All-optical bit memory and optical logic

For the first implementation of photonics into simple chip-scale interconnect, optical memories are probably not required, but we believe that photonic NoC will eventually require more advanced and complicated photonic network functionalities in which optical memory or even optical logic will play an important role. It has been said that a memory or logic function is one of the most difficult tasks for photonics. It is true that it is intrinsically difficult to halt a light signal. Although there has been great progress in achieving slow light or stopped light, the timescale is still limited to less than nanoseconds. Thus, most optical memories have utilised optical bistability in which the state of the optical output exhibits bistability. Fig. 5*a* shows the operating principle of an all-optical bistable memory based on a NL resonator. Optical bistability can be achieved in various systems, including multi-section or coupled lasers and optical NL cavities, but optical memories based on these bistabilities are generally too large in size, intrinsically difficult to integrate and consume too much power (larger than mW) [54, 55].

In 2004 and 2005, we demonstrated all-optical memory action in Si PhC nanocavities [56, 57]. The structure is basically similar to that of the Si all-optical switches described in the previous section, which is unsurprising because, as is well known, all-optical NL cavity-based switches (shown in Fig. 5*a*) should exhibit optical bistability. When a CW bias light is supplied with appropriate power and wavelength detuning, the output intensity can be switched between the ON and OFF states by injecting a set/reset optical pulse. The first realisation of all-optical bistable switching in Si PhC nanocavities was achieved via thermo-optic non-linearity [56], and in 2005 we have achieved a similar operation by employing the much faster carrier-induced optical non-linearity [57].

The power consumption of all-optical bistable memories is mainly determined by the CW bias input power. Generally, the minimum power for all-optical bistable memory operation is deduced from (1) and $U = PQ/\omega$, and is given by

$$P_{\text{bias}} = \frac{\varepsilon_0 \varepsilon n \omega}{2n_2} \frac{V_{\text{cav}}}{Q^2} \tag{3}$$

Equation (3) suggests that a large Q/V_{cav} ratio is advantageous in terms of realising low operation power. Conventional optical bistable memories require a bias power of mW or more, but we have confirmed that all-optical memories in Si PhCs can operate with a bias power of 40 μW for thermo-optic non-linearity and 400 μW for carrier-induced non-linearity. Recently, we applied the same idea to InGaAsP PhC nanocavities since InGaAsP (the band gap wavelength was 1.3 μm) has much larger optical non-linearity as described in the previous section, and we found that the minimum operation power is 40 μW for fast carrier-induced non-linearity [58].

Very recently, we further reduced the operating power by slightly changing the InGaAsP composition (the band gap wavelength was 1.4 μm). The device structure is shown in Fig. 5*b*. The memory operation in InGaAsP PhC nanocavities is shown in Fig. 5*c*. The output light intensity is alternated between ON and OFF by inputting a set pulse and a negative reset pulse. The input wavelength was 1577.75 nm, which was detuned by −0.2 nm from the cavity resonant peak. Since the state of the output is maintained even after the set/reset signals were tuned off, it can memorise a single bit of memory all-optically. The required bias power and set pulse energy were 10 μW and 24 fJ, respectively.

Since the operating power for all-optical bitable memories has been greatly reduced, it may be possible to construct an all-optical random access memory (RAM) by integrating these memories. Although a large-scale optical RAM is still difficult to realise, it may be possible to realise a small-scale optical RAM (around ~Mbyte), which may find applications in certain kinds of information processing circuits.

In addition to allowing us to realise a simple memory function, the integration of optical bistable memories enables us to achieve various optical logic functions. As a simple example, we designed an all-optical flip-flop based on two bistable memories coupled to each other as shown in Fig. 6*a*. This flip-flop functions as a retiming circuit, which corrects the timing jitter of an information bit stream and synchronises it with the clock pulses. This function is normally accomplished by high-speed electronic circuits, but it can be done all-optically in this device. We described

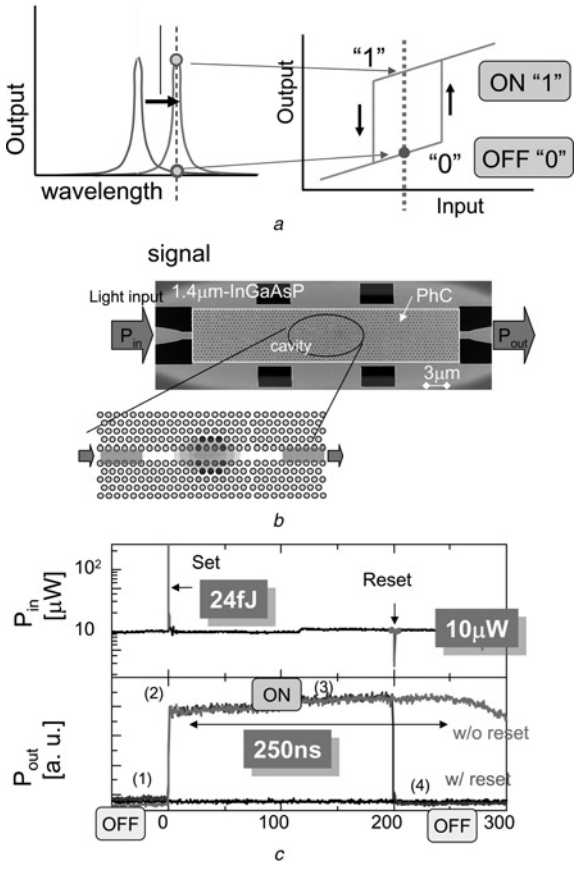

Fig. 5 *All-optical bistable memory based on a* PhC *nanocavity*

a Operating principle of optical bistable memory based on an NL resonator
b Structural design and scanning electron micrograph of an all-optical bistable bit memory in an InGaAsP PhC. The cavity design is the same as that in Fig. 2
c Measured bit memory operation. The state of the output intensity is alternated between ON and OFF by applying set/reset pulses

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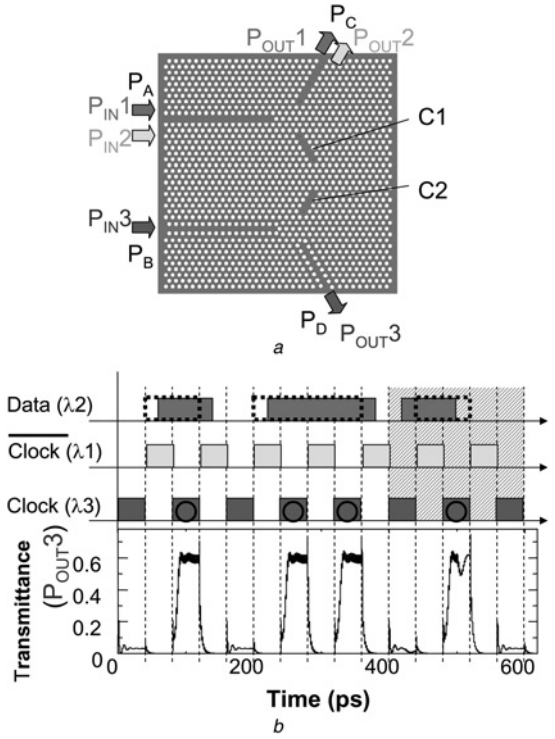

Fig. 6 *All-optical flip-flop consisting of two bistable cavities in a* PhC

a Structural design
b Numerical simulation of flip-flop operation

its operating principle in detail in a previous report [59]. The coupled cavities ($C1$ and $C2$) have one common resonant mode ($\lambda_2 = 1548.48$ nm) extended to both cavities and two modes ($\lambda_1 = 1493.73$ nm, and $\lambda_3 = 1463.46$ nm) localised in each cavity. Here, we use two bistable switching operations for $C1$ and $C2$. The cross feedback is realised as follows. $C1$ is switched ON only when λ_1 and λ_2 are both applied ($P_{IN}1$ and $P_{IN}2$ are ON). $C2$ is switched ON only when λ_3 are applied ($P_{IN}3$ is ON) and simultaneously λ_2 is supplied from $C1$ (which means $C1$ is ON). Thus, the output signal of λ_3 ($P_{OUT}3$) becomes ON only if $P_{IN}3$ is turned ON when $C1$ is already ON. This realises retiming process. We set $P_{IN}1$ and $P_{IN}3$ as two different clock signals, and assume $P_{IN}2$ to be bit stream non-return-to-zero data with finite timing jitter. The resultant $P_{OUT}3$ is precisely synchronised to the clock signals and is actually an RZ data stream converted from $P_{IN}2$ with the jitter corrected. We designed this function in a GaAs PhC, and numerically simulated its operation. Fig. 6*b* shows three input signals (a data stream with jitter, and two clock pulses), and the output from P_D ($P_{OUT}3$). Note that DATA with a solid line indicates the data input with jitter and DATA with a broken line indicates the original data without jitter. As seen in this plot, $P_{OUT}3$ is the RZ signal of the input with the jitter corrected. We confirmed that the operating speed corresponds to 50 GHz operation.

5 Modulator

The previous two sections were devoted to describing typical all-optical devices. In the following sections, we examine electro-optic (E-O) devices that combine CMOS and photonic layers in a photonic NoC. As a first example, we present our recent result for E-O modulators [60]. Fig. 7*a*

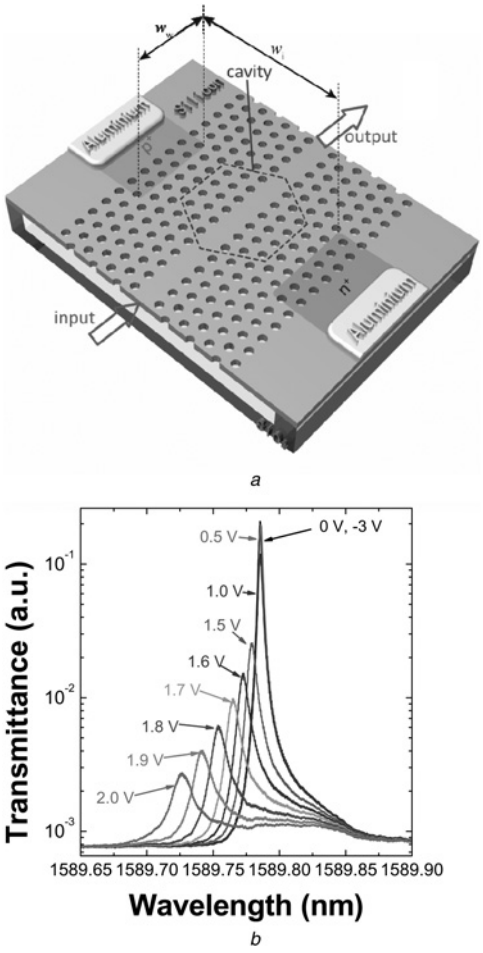

Fig. 7 *E-O modulator based on a Si* PhC *nanocavity with a p−i−n junction*

a Schematic of a fabricated modulator based on a Si PhC nanocavity with a $p-i-n$ junction. The cavity design is the same as that in Fig. 2
b Measured transmission spectra at various applied voltages

shows an E-O modulator based on a Si PhC nanocavity. The cavity is a width-modulated line-defect cavity, which is the same as that shown in Fig. 2. This cavity is integrated with input/output waveguides and is equipped with a $p-i-n$ junction. By applying voltage across the $p-i-n$ junction, we can modulate the intensity of a light signal transmitted across the cavity. The mechanism is similar to the all-optical switching shown in Fig. 3, but the switching operation is now performed electrically. Similar E-O modulators in Si have been extensively studied in the silicon photonics community, in which ring resonators with a diameter of around 10 μm or more have been employed [61]. The key to our device is that we can make use of the large Q/V ratio of PhC nanocavities to reduce the driving power and footprint.

A major technological challenge as regards constructing photonic-crystal E-O modulators is to fabricate $p-i-n$ junctions without degrading the cavity's Q since both the p and n regions have substantial absorption loss. We carefully determined an appropriate geometrical design for a $p-i-n$ junction, and achieved an ultrahigh-Q nanocavity (Q of 0.5∼0.8 million) coexisting with a lateral $p-i-n$ junction. The $p-i-n$ junction was formed by ion implantation and the details are described in [60]. To the best of our knowledge, this is the first realisation of a PhC nanocavity with a lateral $p-i-n$ junction. As shown in Fig. 7*b*, the cavity resonance was shifted to shorter wavelengths by

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applying a forward voltage of 1–2 V, which is explained by the plasma dispersion carrier injection into the cavity. A modulation contrast of 14.2 dB was achieved for the device with a loaded Q of 0.54 million at an applying voltage of 1.5 V, where the measured current into the device was 1.4 μA. Thus, the electrical power required for modulation is as small as 2.1 μW. This value is about 4.6 times smaller than that reported for a Si micro-ring resonator E-O modulator [61].

The electrical power required for modulation P_{mod} is determined in a similar way to the case for carrier-induced all-optical switching (2). First, the required carrier density is estimated from the relation $1/Q = \Delta n/n = \sigma N/n$ and then the required current is given by

$$I_{\mathrm{mod}} = \frac{eN_{\mathrm{mod}}V_{\mathrm{c}}}{\Gamma\tau_{\mathrm{c}}} = \frac{en}{\sigma\tau_{\mathrm{c}}}\frac{V_{\mathrm{c}}}{\Gamma Q} \simeq \frac{en}{\sigma\tau_{\mathrm{c}}}\frac{V}{Q} \tag{4}$$

where e is an elemental charge, τ_{c} is the carrier lifetime, and V_{c} is the effective volume within which carriers are distributed. V in the last term represents $\max(V_{\mathrm{c}}, V_{\mathrm{cav}})$. Γ is a confinement factor that represents the overlap between the light field and carrier distribution, and is unity when the carrier distribution is wider than the field distribution, which is the case in the present situation [the last equation in (4)]. If this is not the case, Γ is approximately given by $V_{\mathrm{c}}/V_{\mathrm{cav}}$, and we must substitute V_{c} with V_{cav} in the following argument. When we take account of the fact that the operating voltage is restricted by the energy bandgap of the material (which cannot be largely altered), the electric power required for modulation is basically scaled as V_{c}/Q. V_{c} is approximately given by the size of the i region of the $p-i-n$ junction. Since V_{c} is restricted by the geometrical cavity size, we can expect small V_{c} for PhC nanocavities. In our case, V_{c} is approximately $0.2 \times 2.5 \times 4.4\ \mu\mathrm{m}^3 = 2.2\ \mu\mathrm{m}^3$, which is apparently much smaller than that in Si micro-ring resonator devices [61]. Hence, large Q/V_{cav} for PhC nanocavities is again advantageous for low power operation.

For the same device, we demonstrated successful E-O modulation up to a repetition frequency of 0.5 GHz. The speed of our present device is currently not limited by the cavity photon lifetime (~300 ps) but by some imperfection in the $p-i-n$ junction. For high-speed operation (after resolving the issue of $p-i-n$ fabrication), we may need finally to sacrifice Q, but the smallness of our PhC nanocavities is always advantageous over other types of cavities. It is worth noting that the capacitance of our device is extremely small (~10 aF) also because of the smallness of the device, which may be advantageous for high-speed operation in future. Although we presented our demonstration of modulators based on Si, the same scenario may be applied for device based on III/V materials.

6 Receiver

A photo detector (receiver) is another important element for E-O conversion between the CMOS and photonic layers in photonic NoC. To fabricate an efficient receiver integrated with other devices in a chip, it is essentially important to realise high absorption efficiency in the receiver and low absorption loss outside the receiver, simultaneously. There are several ways to achieve this condition. The most straightforward way is to replace a transparent material with an absorptive material only within a receiver. This is normally accomplished for compound semiconductor devices by a combination of etching-and-regrowth processes. However, the regrowth interface usually produces a large dark current, which could be fatal for nanophotonic receivers which have to detect small signal efficiently.

Recently, we have proposed and demonstrated a novel way to construct a photo-receiver without an etching-regrowth process, by which highly sensitive photo-detectors are made only of pure silicon without any substitution or reformation of materials [62]. Light detection of light at 1.55 μm was achieved by TPA in silicon (note that silicon is transparent at 1.55 μm). Since TPA is based on the third-order optical non-linearity of materials, its absorption efficiency is very low. As was discussed in Section 3, however, we can dramatically enhance the efficiency of optical NL processes (the TPA process in this case) in high-Q PhC nanocavities. Thus, optical absorption occurs only in the cavity even if we employ a single material for the whole device. This design should lead to small dark current.

The device structure is essentially the same as that used for Si E-O modulators that consist of high-Q nanocavities with $p-i-n$ junctions (Fig. 7*a*). We confirmed that sizable photocurrent appears when the $p-i-n$ was reverse biased at −3 V and 1.55 μm light was injected via the input waveguide. Fig. 8 shows the measured photocurrent as a function of the input optical power. The onset of TPA is clearly seen even at an optical input of 10 nW, which is well explained by a theoretical calculation including the TPA in Si. At around a 100 nW–10 μW input, the quantum efficiency is close to 10%, which means that 20% of the input photons were converted to electrons via the TPA process. If we take the cavity–waveguide coupling efficiency into account, 44% of light in the cavity was absorbed via the TPA process, which is a surprisingly high value. The most notable feature of this detector is its dark current, which is as small as 15 pA when the detector is operating. This value is much smaller than that for conventional photo-detectors at 1.55 μm including III/V, Ge/Si or ion-implanted Si. This is because we did not rely on regrowth or implantation processes which may damage the crystal quality.

The TPA detection efficiency is given by the following approximate relation [63]

$$\eta_{\mathrm{eff}} \simeq \alpha_{\mathrm{TPA}}\tau_{\mathrm{ph}} = \beta_{\mathrm{TPA}}Iv_g\tau_{\mathrm{ph}} = \beta_{\mathrm{TPA}}v_g^2\frac{U_{\mathrm{cav}}}{V_{\mathrm{cav}}}\tau_{\mathrm{ph}}$$
$$= \frac{\beta_{\mathrm{TPA}}v_g^2}{\omega^2}\frac{Q^2}{V_{\mathrm{cav}}}P_{\mathrm{in}} \simeq 5\times10^{-6}\frac{Q^2}{V_{\mathrm{cav}}(n/\lambda)^3}P_{\mathrm{in}} \tag{5}$$

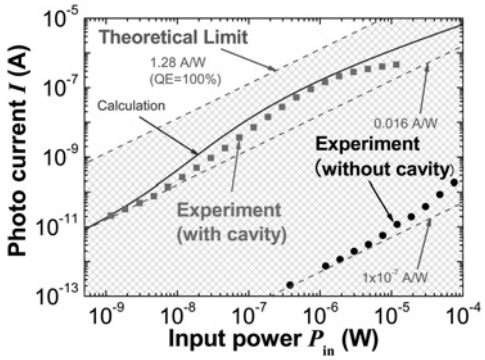

Fig. 8 *Si TPA photo-detector based on a Si PhC nanocavity with a $p-i-n$ junction*
The device structure is the same as that in Fig. 7. The plot shows the measured photocurrent as a function of the input power

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where α_{TPA}, β_{TPA}, τ_{ph}, I are the TPA rate, the TPA coefficient, the photon lifetime in the cavity and the light intensity in the cavity, respectively. The final equation was obtained by assuming typical β_{TPA} for Si (0.9 cm/GW). Equation (5) tells us that if the cavity Q and volume are a few times 10^5 and $\sim(\lambda/n)^3$, the TPA efficiency becomes of the order of unity at the input power of μW level, which explains our result.

Recently, there have been extensive studies concerning photo-receivers on Si for telecommunication wavelengths (~1.55 μm) in silicon photonics application. For this purpose, Ge detectors have been successfully demonstrated on a Si platform, which are integrated with silicon waveguides by hetero-epitaxial growth [64]. Alternatively, part of the silicon was ion implanted so as to produce absorption centres as a result of defect formation, which provides a sensitive photo-detector at 1.55 μm [65]. However, both methods inevitably degrade the crystal quality, which results in substantially high dark current (170 nA for Ge/Si [64] and 0.5 nA for implanted Si [65]).

Although we employed silicon in our study shown here, the same scenario can be applied for InGaAsP materials. Then, we may be able to form extremely low dark current photo-detectors with much higher efficiency because TPA efficiency is over a magnitude larger for InGaAsP than for Si. The penalty for this TPA detector is its narrower bandwidth which may not be favoured for some applications. Recent IBM's demonstration [66] of novel nano-scale metal-semiconductor-metal avalanche photo-diodes based on Ge/Si showed excellent performance in terms of the speed, bandwidth and gain, although the dark current is still rather high (~50 μA).

7 Lasers

As a last example of nanophotonic devices, we briefly examine a laser. For photonic NoC applications, we must reduce the threshold power for (electrical or optical) pumping lasers, since conventional lasers consume several pJ at 25 Gbit/s operation [6, 7]. In addition, these lasers should be integrated with output waveguides. As we will see in the below, PhC nanocavities are advantageous for reducing the lasing threshold (and intrinsically suited for integration as discussed in previous sections). It has sometimes been pointed out that the output light intensity from PhC nanocavity lasers is too small for many applications. However, high output power is not required for photonic NoC applications.

Here we briefly examine the laser threshold in PhC nanocavities. The laser threshold current (in the linear gain regime) is generally given by [67]

$$I_{th} = \frac{eN_{th}V_c}{\tau_c} = \frac{eV_c}{\tau_c}\left(\frac{\omega}{\Gamma g' Q} + N_0\right) \simeq \frac{e}{\tau_c}\left(\frac{\omega V}{g' Q} + N_0 V_c\right) \quad (6)$$

where N, N_0, v_g and g' are, respectively, the carrier density, the transparent carrier density, the group velocity of light and the differential gain rate [the conventional gain is given by $g' v_g(N - N_0)$]. V in the last term represents $\max(V_c, V_{cav})$. This equation tells us that if we intend to reduce the threshold, we must employ a device with higher Q and smaller V_c and V_{cav}. Equation (6) appears similar to (4), showing that large Q/V is favourable as regards reducing the operating power. Thus, we can expect a significant reduction of the threshold in PhC nanocavities.

However, the presence of the last term in (6) suggests that it is also important for lasers to reduce V_c. In other words, we need to introduce effective carrier confinement mechanisms. In fact, this has been an issue for laser application of PhC nanocavities since the carrier confinement is not always satisfactory in PhC structures. One way of achieving strong carrier confinement is to employ quantum dots for an active material with a very small volume. Very small threshold power (~2.5 μW) for room-temperature CW lasing operation was reported for quantum dot PhC nanocavity lasers [68]. Another way is to introduce a buried heterostructure into a PhC cavity. We have recently fabricated a PhC laser structure with an ultrasmall gain region embedded within a transparent cavity by using the etching-and-regrowth technique [69, 70].

Most of PhC nanocavity lasers have been operated by optical pumping. Although optically pumped lasers may be useful in various situations in the photonic layer in photonic NoC, electrically pumped lasers may also be useful for E-O conversion between the CMOS and photonic layers. To date, there has been only one report on electrically pumped PhC nanocavity lasers [71], and current injection is probably the most important challenge as regards PhC nanocavity lasers.

8 Outlook

In this article we have shown that we can reduce the footprint and driving power/energy of a variety of photonic devices by employing PhCs. These photonic-crystal-based nanophotonic devices are ~μm order in size and are suited for integration in a chip. The consumption power and energy have been substantially reduced compared with conventional photonic devices. The results indicate that these devices are promising candidates as key components for realising photonic NoC. However, there are still a number of issues to be dealt with if we are to achieve this goal. In this last section, we comment on the detached positioning of these nanophotonic devices for future NoC applications among other ongoing studies, and mention what needs to be done next for these photonic-crystal-based nanophotonic devices.

There are many approaches for introducing optics into an electronics chip. Most current research activity is concentrated on simple optical interconnects, and the approaches are mostly based on silicon photonics. Our aim with PhCs is to realise more complicated functions rather than simple interconnects, and to introduce large-scale photonic integration. To accomplish this, we must adopt a novel approach, such as the use of PhCs (or perhaps plasmonics, or even their combination). Thus, the demand for photonic-crystal-based nano-photonics fully depends on how widely/deeply we may have to introduce optics into a chip. In fact, whether or not a simple optical interconnect in a chip would pay is still under discussion [3, 5], and therefore the need for more complicated optics is rather unclear at present. However, in principle, we believe that the energy cost of electronics information processing on any size scale will ultimately be dominated by the energy needed for transmitting signals between processing devices as the processing bandwidth increases. Therefore we may have to introduce extremely dense optical interconnect closely incorporated with electronics circuits or we may have to replace part of the electronic circuits with photonic circuits, both of which are far beyond simplistic optical interconnects. Hence, if we could establish an effective

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scheme for introducing an intelligent photonic network based on a certain level of photonic integration on an electronic chip, an appropriate entangled combination of electronics information processing and photonics information processing would constitute a final solution for a chip. Photonic-crystal-based nano-photonic components are one of the most promising candidates for this final target.

The current studies described in this manuscript only concern the operation of each device, but we definitely need to develop ways of realising cooperative operation (photonic–electronic/photonic–photonic) as the next step. Concerning photonic–electronic cooperation, the most urgent requirement is too establish ways of injecting current and applying voltage in PhCs. Another issue is to find a way to combine a photonic layer and a Si CMOS. Currently, we regard that if we pursue a sophisticated functional dense photonic layer, we should use III/V semiconductors (probably based on InGaAsP) for a base material of the photonic layer rather than silicon (although some of our works given in this manuscript were based on silicon). Then, we may employ a wafer-scale bonding technique [72–74] for this purpose, by which we can overlay a III/V semiconductor PhC layer on a Si CMOS. Concerning photonic–photonic cooperative operation, it is already possible to integrate several photonic devices connected by waveguides in PhCs. Thus, some demonstration of photonic network operation in PhCs might be possible in the near future. When the degree of integration further increases, finite reflection at each component may become a problematic issue, which is especially serious for analogue devices. Thus, we think that photonic digital processing including 3R operation will be finally needed (this is the reason why we are interested in optical bistability). Of course, the requirement for the fabrication accuracy and reproducibility will become also more severe as the degree of integration increases, and we will definitely need to improve the fabrication process of those photonic nanodevices.

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